WHAT IS CLAIMED IS:

1. A process variable transmitter, comprising:

a first phase-locked loop having a first bandwidth producing a first output signal, and operable to lock into a frequency of an input signal;

a second phase-locked loop having a second bandwidth narrower than the first bandwidth, producing a second output signal, and operable to lock into the frequency of the input signal with greater accuracy and greater immunity to noise than the first phase-locked loop; and

a switch operable to switch an output signal of the process variable transmitter between the first output signal and the second output signal.

2. The process variable transmitter of claim 1 wherein

the second phase-locked loop generates a lock indicator signal when the second phase-locked loop is locked into the frequency of the input signal, and

the switch switches between the first output signal and the second output signal based on a status of the lock indicator signal.

3. The process variable transmitter of claim 1 wherein at least one of the first phase-locked loop and the second phase-locked loop comprises:

a phase sensitive detector operable to receive the input signal and to produce a detector output signal;

a loop filter operable to receive the detector output signal and to produce a filtered signal; and

a voltage controlled oscillator operable to receive the filtered signal and to produce an oscillator signal,

wherein the phase sensitive detector is further operable to receive the oscillator signal as a feedback signal of the at least one of the first phase-locked loop and the second phase-locked loop.

4. The process variable transmitter of claim 3 wherein the switch and each of the phase sensitive detector, the loop filter and the voltage controlled oscillator of at least one of the first and second phase-locked loops are implemented in a software process.

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5. The process variable transmitter of claim 4 wherein the switch and each of the phase sensitive detector, the loop filter and the voltage controlled oscillator of at least one of the first and second phase-locked loops is implemented in the software process on a single digital signal processor chip.

6. The process variable transmitter of claim 3 wherein the phase sensitive detector of at least one of the first and second phase-locked loops comprises a Hilbert transformer.

7. The process variable transmitter of claim 6 wherein the at least one of the first and second phase-locked loops comprises a heterodyning module operable to heterodyne the input signal prior to processing the input signal with the Hilbert transformer.

8. The process variable transmitter of claim 1 further comprising an amplitude detector operable to sense an amplitude of the input signal and to generate a low flow signal when the amplitude of the input signal is below a user-controlled value.

9. The process variable transmitter of claim 8 further comprising a pre-filter operable to filter the input signal prior to processing by at least one of the first phase-

locked loop and the second phase-locked loop, and wherein, based on a status of the low flow signal,

a fixed center frequency of the second phase-locked loop is switchable between the first output signal and $2\pi f_{ph}$, where f_{ph} is a high cut-off frequency of the pre-filter,

the pre-filter is switchable between an ON state and an OFF state, and

the switch switches the output signal of the process variable transmitter to the second output signal.

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10. The process variable transmitter of claim 1 further comprising a self-validating module operable to generate validated uncertainty parameters including a measurement value and an uncertainty value relating to the quality of the measurement value.

11. The process variable transmitter of claim 10 wherein the validated uncertainty parameters generated by the self-validating module include a measurement status variable.

12. The process variable transmitter of claim 10 wherein the self-validating module is implemented in a software process.

13. The process variable transmitter of claim 1 wherein the process variable transmitter comprises a vortex flowmeter.

14. A vortex flowmeter comprising:

a flow sensor operable to sense pressure variations due to vortex-shedding of a fluid in a passage and to convert the pressure variations to a flow sensor signal, in the form of an electrical signal having sinusoidal characteristics; and

a signal processor operable to receive the flow sensor signal and to generate an output signal corresponding to the pressure variations due to vortex-shedding of the fluid in the passage, the signal processor comprising:

phase-locked loops (PLLs) having different characteristics from each other and operable to receive the flow sensor signal and lock onto the flow sensor signal, and produce PLL output signals indicative of the flow sensor signal, and

a switch for switching the output signal generated by the signal processor from among the PLL output signals..

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15. The vortex flowmeter of claim 14 wherein the signal processor is implemented by a software process in a digital signal processor chip.

16. The vortex flowmeter of claim 14 wherein a first one of the PLLs is operable to lock onto the flow sensor signal faster than any other PLL, and a second one of the PLLs is operable to lock onto the flow sensor signal with greater accuracy and greater immunity to noise than the first PLL.

17. The vortex flowmeter of claim 16 wherein the switch switches the output signal generated by the signal processor from an output signal of the first PLL to an output signal of the second PLL when the second PLL locks onto the flow sensor signal.

18. The vortex flowmeter of claim 14 further comprising an amplitude detector operable to detect an amplitude of the flow sensor signal, wherein the amplitude detector generates a low flow signal when the amplitude of the flow sensor signal is below a user-controlled value.

19. The vortex flowmeter of claim 18 further comprising a filter operable to filter the flow sensor signal prior to processing by the slow PLL.

20. The vortex flowmeter of claim 19 wherein the filter is switchable between an ON state and an OFF state, and is switched to the ON state based on the low flow signal.

21. A method of determining a flow rate sensed by a vortex flowmeter, the method comprising:

inputting to a signal processor an input signal having sinusoidal characteristics, the signal processor comprising a first phase-locked loop (PLL) having a first bandwidth and a second PLL having a second bandwidth narrower than the first bandwidth;

locking into the frequency of the input signal using the first PLL, the first PLL having a fast loop filter having a large natural frequency to enable the first PLL to lock quickly into the frequency of the input signal;

locking into the frequency of the input signal accurately using the second PLL, the second PLL having a slow loop filter having a small natural frequency to enable the second PLL to lock into the frequency of the input signal more accurately and with greater immunity to noise than the first PLL;

generating a lock indicator signal when the second PLL is locked into the frequency of the input signal; and

switching an output of the signal processor from between an output signal produced by the first PLL and an output signal produced by the second PLL based the lock indicator signal.

22. The method of claim 21 wherein switching the output of the signal processor comprises switching the output of the signal processor from the output signal of the first PLL to the output signal of the second PLL when the lock indicator signal indicates that the second PLL is locked into the frequency of the input signal.

23. The method of claim 21 further comprising providing the output signal of the first PLL to the second PLL as an initial condition frequency of the second PLL to assist lock-in by the second PLL.

24. The method of claim 21 further comprising switching the output of the signal processor from the from the second PLL output signal of the second PLL to the output signal of the first PLL when the lock indicator signal indicates that the second PLL is out of lock with the frequency of the input signal.

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25. A signal processing apparatus for acquiring a frequency of an input signal, the apparatus comprising:

a first phase-locked loop operable to lock into the frequency of the input signal;

a first lock indicator for generating a first lock indicator signal based on whether the first phase-locked loop is locked into the frequency of the input signal;

a self-validating module operable to generate validated uncertainty parameters based on the first lock indicator signal, wherein the validated uncertainty parameters include a measurement value corresponding to the output signal and an uncertainty value relating to the quality of the measurement value.

26. The signal processing apparatus of claim 25 further comprising:

a second phase-locked loop operable to lock into the frequency of the input signal; and

a second lock indicator for generating a second lock indicator signal based on whether the second phase-locked loop is locked into the frequency of the input signal,

wherein the self-validating module is operable to generate validated uncertainty parameters based on the first and second lock indicator signals.

27. The signal processing apparatus of claim 25 wherein the validated uncertainty parameters generated by the self-validating module include a measurement status variable.